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## Seventh Semester B.E. Degree Examination, Feb./Mar. 2022 DSP Algorithms and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

## PART - A

1 a. An analog signal is sampled at the rate of 8KHz. If 512 samples of signals are used to compute DFT X[k], determine the analog and digital frequency spacing between adjacent X[k] elements. Also, determine analog and digital frequencies corresponding to k = 64.

(06 Marks)

b. Explain the need of decimation and interpolation in DSP systems.

(06 Marks)

c. Find the interpolated sequence, if  $x(n) = (0 \ 3 \ 6 \ 9 \ 12)$ ,  $b_k = \left[\frac{1}{3}, \frac{2}{3}, 1, \frac{2}{3}, \frac{1}{3}\right]$  and interpolation factor is 3. (08 Marks)

What is the need of shifter in DSP? Explain the implementation of 8-bit right shift barrel

shifter with a diagram. (12 Marks)

b. Explain special addressing modes with neat diagrams.

(06 Marks)

- c. The 256 products of 16-bits are to be summed up in a MAC unit, how many guard bits should be provided to prevent overflow? (02 Marks)
- 3 a. Draw and explain the functional diagram of multiplier/adder unit of TMS320C54XX processors. (06 Marks)
  - b. With a neat block diagram, explain direct addressing mode for TMS320C54XX. (06 Marks)
  - c. Draw a neat diagram for page 0 of program and data memory in microprocessor and micro computer mode. (08 Marks)
- 4 a. Explain the operation of the following instructions of TMS320C54XX processor
  - i) MPY[R] S<sub>mem</sub>, dst
  - ii) MACD S<sub>mem</sub>, pmad, src
  - iii) MAS X<sub>mem</sub>, Y<sub>mem</sub>, src, dst
  - iv) LD  $S_{mem}$ , 16, dst.

(08 Marks)

- b. Show the pipeline operation of the following sequence of instructions, if the initial value of AR3 is 80 and the values stored in memory location 80, 81, 82 are 1, 2 and 3
  - LD \*AR3+, A

ADD # 1000H, A

STL A, \*AR3+

(06 Marks)

c. Describe the operation of hardware timer with neat diagram.

(06 Marks)

## PART-B

- 5 a. Obtain decimal value of the following Q<sub>15</sub> numbers
  - i) 8D1CH
  - ii) 0D67H
  - iii) D0B5H
  - iv) FFFFH

v) 4E68H.

b. Explain with a neat diagram, equations, algorithm and program for FIR filter implementation using TMS320C554XX processor.

(10 Marks)

(10 Marks)

- 6 a. Explain overflow and scaling in butterfly computation. (06 Marks)
  b. Derive scaling factor for DIF FFT butterfly structures. (06 Marks)
  c. Draw 8-point DIT FFT structure with scaling factor. (08 Marks)
- a. Design a data memory system with address range 000800H 000FFFH for a TMS320C5416. Use 2K × 8 RAM memory chips. (10 Marks)
   b. With a neat flowchart explain the response of digital signal processor for input/output in

interrupt mode. (10 Marks)

- Write short notes on:
  - a. DSP based telemetry receiver
  - b. Codec Interface
  - d. Speech Processing System
  - c. Image Processing System.

(20 Marks)